CCS Technical Documentation
NPM-8 Series Transceivers

3. System Module

Issue 1 07/2002

Contents

Transceiver NPM-8

Introduction

This section specifies the baseband module for the NPM-8 transceiver. The baseband module includes the baseband engine chipset, the UI components, and the acoustical parts for the transceiver.

NPM-8 is a handportable, dualband GSM 850/1900 phone, with GPRS for the Basic/ Expression segment, using DCT4 generation baseband (UEM/UPP) and RF (MJOELNER) circuitry.

NPM-8 supports both three- and two-wire type DCT3 chargers. Three-wire chargers are treated like two-wire types. There is no separate PWM output; the third wire is connected to ground.

The BLC-1 Li-ion battery is used as the main power source for NPM-8. The BLC-1 has a nominal capacity of 825 MAh.

Hardware characteristics

- Hi-Res (96x65) illuminated B&W display
- ESD-proof keymat
- Support for internal semi-fixed batteries (Janette type)
- Audio amplifier and SALT speaker for MIDI support
- Internal vibra
- Supports voice dial activation via headset button
- DC out feature for supporting electrical A-covers
- Support for both Li-ion and NiMH batteries

Note: 5V SIM cards are no longer supported by DCT-4 generation baseband.

Technical Summary

The baseband module contains two main ASICs (UEM and UPP). The baseband module also contains an audio amplifier for MIDI support and a 64-Mbit Flash IC. The baseband is based on the DCT4 engine program.

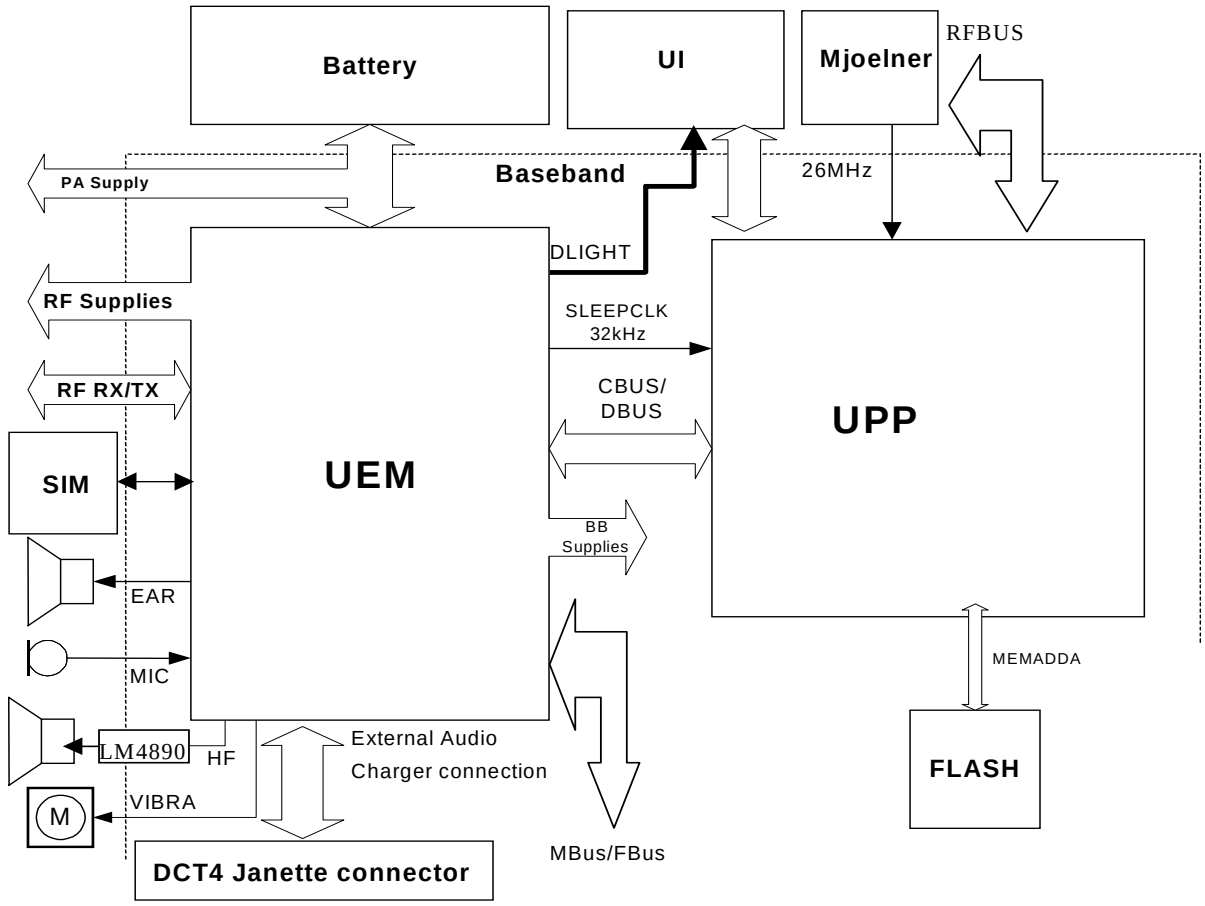


Figure 1: NPM-8 baseband block diagram

The UEM supplies both the baseband module as well as the RF module with a series of voltage regulators. Both the RF and Baseband modules are supplied with regulated voltages of 2.78V and 1.8V. The UEM includes six linear LDO (low drop out) regulators for baseband and seven regulators for RF, the BB regulator VFLASH1, RF regulators VR1B, VR4 as well as the current sources (IPA1 and IPA2 must be kept disabled by SW as they are left disconnected on the PWB). The UEM also supplies the baseband SIM interface with a programmable voltage of either 1.8V or 3.0V. The UPP core is supplied with a programmable voltage of 1.0V, 1.3V, 1.5V, or 1.8V.

The UPP operates from a 26MHz clock, coming from the RF ASIC Mjoelner. The 26 MHz clock is internally divided by two, to the nominal system clock of 13 MHz.

The UEM contains a real-time clock, developed from the 32.768 MHz crystal oscillator. The 32.768 MHz clock is fed to the UPP as a sleep clock.

The communication between the UEM and the UPP is done via the bidirectional serial busses, CBUS and DBUS. The CBUS is controlled by the MCU and operates at a speed of 1 MHz. The DBUS is controlled by the DSP and operates at a speed of 13 MHz. Both processors are located in the UPP.

The interface between the baseband and the RF section is mainly handled by the UEM

ASIC. UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signals and also A/D and D/A conversions of received and transmitted audio signals to and from the user interface. The UEM supplies the analog signals to the RF section according to the UPP DSP digital control. The RF ASIC Mjoelner is controlled through UPP RFBUS serial interface. There also are the separate signals for PDM-coded audio. Digital speech processing is handled by the DSP inside the UPP ASIC. The UEM ASIC is a dual-voltage circuit supplying the digital section with 1.8 V and the analog section with 2.78 V. VBAT is also used in some blocks.

The baseband supports both internal and external microphone inputs and speaker outputs. Input and output signal source selection and gain control is handled by the UEM according to control messages from the UPP. Keypad tones, DTMF, and other audio tones are generated and encoded by the UPP and transmitted to the UEM for decoding. NPM-8 has two external control interfaces: FBUS and MBUS. The serial control interfaces can be accessed through the test pads located in the battery area.

Technical Specifications

Operating conditions - Temperature Conditions

Table 1: Temperature conditions for NPM-8

Environmental conditions	Ambient temperature
Normal operation	-25° C ... +55° C
Reduced performance	-40° C ...-25° C and +55° C ... +85° C

Absolute Maximum Ratings

Table 2: Absolute maximum ratings

Signal	Rating
Battery voltage	-0.3 ... 5.4V
Charger input voltage	-0.3 ... 20V

DC Characteristics

Regulators and Supply Voltage Ranges

Table 3: Battery voltage range

Signal	Min	Nom	Max	Note
VBAT	3.1 V	3.6 V	4.235 V	3.1 V SW cut off

Table 4: BB regulators

Signal	Min	Nom	Max	Note
VANA	2.70 V	2.78 V	2.86 V	I_{max} = 80 mA
VFLASH1	2.70 V	2.78 V	2.86 V	I_{max} = 70 mA I_{Sleep} = 1.5 mA
VFLASH2	2.70 V	2.78 V	2.86 V	Not used
VSIM	1.745 V 2.91 V	1.8 V 3.0 V	1.855 V 3.09 V	I_{max} = 25 mA I_{Sleep} = 0.5 mA
VIO	1.72 V	1.8 V	1.88 V	I_{max} = 150 mA I_{Sleep} = 0.5 mA
VCORE	1.0 V 1.235 V 1.425 V 1.710 V	1.053 V 1.3 V 1.5 V 1.8 V	1.106 V 1.365 V 1.575 V 1.890 V	I_{max} = 200 mA I_{Sleep} = 0.2 mA Used voltages: (c015) = 1.8 V (c035) = 1.5 V

Table 5: RF regulators

Signal	Min	Nom	Max	Note
VR1A	4.6 V	4.75 V	4.9 V	I_{max} = 10 mA
VR1A	4.6 V	4.75 V	4.9 V	Not used
VR2	2.70 V 3.20 V	2.78 V 3.3 V	2.86 V 3.40 V	I_{max} = 100 mA
VR3	2.70 V	2.78 V	2.86 V	I_{max} = 20 mA
VR4	2.70 V	2.78 V	2.86 V	Not used
VR5	2.70 V	2.78 V	2.86 V	I_{max} = 50 mA I_{Sleep} = 0.1 mA
VR6	2.70 V	2.78 V	2.86 V	I_{max} = 50 mA I_{Sleep} = 0.1 mA
VR7	2.70 V	2.78 V	2.86 V	I_{max} = 45 mA

Table 6: Current sources

Signal	Min	Nom	Max	Note
IPA1 and IPA2	0 mA	-	5 mA	Not used

Internal Signals and Connections

The following tables describe internal signals. The signal names can be found on the schematic for the EN9 PWB.

Audio

Table 7: Internal microphone

Signal	Min	Nom	Max	Condition	Note
MIC1P (Differential input P)	-	-	100 mV_{pp}	G=20 dB	1kΩ to MIC1B (RC filtered by 470R/22uF)
MIC1N (Differential input N)	-	-	100 mV_{pp}	G=20 dB	1kΩ to GND
MIC1B (Microphone Bias)	2.0 V	2.1 V	2.25 V	DC	
External loading of MICB1	-	-	600 uA	DC	

Table 8: Internal speaker (Differential output EARP & EARN)

Signal	Min	Nom	Max	Condition	Note
Output voltage swing	4.0	-	-	Vpp	Differential output
Load Resistance (EARP to EARN)	26	32	-	W	
Load Capacitance (EARP to EARN)	-	-	50	nF	

MIDI

Table 9: Connections between UPP and LM4890

Signal	From	To	Parameter	Min	Max	Unit	Notes
Shutdown	GENIO[14]	Shutdown	Vih Vil	1.2 -	- 0.4	V V	LM4890 detections thresholds levels

Table 10: Connections between UEM/Battery and LM4890

Signal name	From	To	Parameter	Min	Max	Unit	Notes
XAUDIO[1] Filtered signal	UEM, HF No direct connection between UEM and LM4890	LM4890	Output Swing	1.0	-	Vpp	with 60 dB signal to total distortion ratio
VBAT	Battery	LM4890	Supply	3.1	4.2	V	Lower limit is SW cut-off

LCD

Table 11: LCD connector interface

Pin	Signal	NMP net	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	/RES	XRES		Reset	-	-	0.3 x V_{DDI}	V	Logic Low, active
			t_{rw}		1000	-	-	ns	For valid reset
2	/SCE	XCS		Chip Select	0.7 x V_{DDI}	-	-	V	Logic High
					-	-	0.3 x V_{DDI}	V	Logic Low, active
			t_{S2}		60	-	-	ns	Setup time
			t_{H2}		100	-	-	ns	Hold time
3	VSS	VSS	GND	Ground	-	0	-	V	
4	SDATA	SDA		Input	0.7 x V_{DDI}	-	-	V	Logic High
					-	-	0.3 x V_{DDI}	V	Logic Low
				Output @ I_{OL} = 0.5mA, I_{OH} = -0.5mA	0.7 x V_{DDI}	-	-	V	Logic High
					-	-	0.3 x V_{DDI}	V	Logic Low
			t_{s1}		100	-	-	ns	Data setup time
			t_{H1}		100	-	-	ns	Data hold time
5	SCLK	SCLK		Serial clock input	0.7 x V_{DDI}	-	-	V	Logic High
					-	-	0.3 x V_{DDI}	V	Logic Low
			t_{cyc}		153,8	-	-	ns	Serial clock cycle (max. 4 MHz)
			t_{PWH1}		50	-	-	ns	Serial clock high pulse width
			t_{PWL1}		50	-	-	ns	Serial clock low pulse width
6	VDD_1	VDDI		VDD digital power supply	1.72	1.8	1.88	V	
7	VDD_{2in}	VDD		Booster power supply	2.6	2.78	2.86	V	VFLASH1
8	$VLCD-_{out}$	VOUT		Booster output	-	-	12	V	Decoupled to GND on PCB with 1uF

Baseband – RF interface

Table 12: BB – RF interface description

Signal name	From	To	Parameter	Min.	Typ.	Max.	Unit	Notes
RFICCNTRL (2:0)			MJOELNER/BIFROST control bus					
RFBUSEN1X	UPP	MJOEL-NER	Logic "1"	1.38	-	1.80	V	RF Chip select
			Logic "0"	0	-	0.4	V	
RFBUSDA	UPP	MJOEL-NER	Logic "1"	1.38	-	1.80	V	RF serial control bus (bi-directional)
			Logic "0"	0	-	0.4	V	
RFBUSCLK	UPP	MJOEL-NER	Logic "1"	1.38	-	1.80	V	RF bus clock
			Logic "0"	0	-	0.4	V	
Clock			System clock for phone					
RFCLK	MJOELNER	UPP	Frequency	-	26	-	MHz	System clock UPP minimum recommended amplitude is 0.3Vpp. Waveform: Sinus/ triangle
			Signal amplitude	0.3	1	1.376	Vpp	
			Duty cycle (Mjoelner spec.)	40	-	60	%	
RFCONV (9:0)			RF / BB analogue signals					
RXIINP	MJOELNER	UEM	Voltage swing	1.35	1.4	1.45	V	Positive in-phase Rx signal
			DC level	1.3	1.35	1.4	V	
			I/Q amplitude mismatch	-	-	0.2	dB	
			I/Q phase mismatch	-5	-	5	Deg.	
			Data clock rate	-	-	13	MHz	
RXIINN	MJOELNER	UEM	Voltage swing	1.35	1.4	1.45	V	Negative in-phase Rx signal
			DC level	1.3	1.35	1.4	V	
			I/Q amplitude mismatch	-	-	0.2	DB	
			I/Q phase mismatch	-5	-	5	Deg.	
			Data clock rate	-	-	13	MHz	

RXQINP	MJOELNER	UEM	Voltage swing	1.35	1.4	1.45	V	Positive quadrature phase RX signal
			DC level	1.3	1.35	1.4	V	
			I/Q amplitude mismatch	-	-	0.2	dB	
			I/Q phase mismatch	-5	-	5	Deg.	
			Data clock rate	-	-	13	MHz	
RXQINN	MJOELNER	UEM	Voltage swing	1.35	1.4	1.45	V	Negative quadrature phase RX signal
			DC level	1.3	1.35	1.4	V	
			I/Q amplitude mismatch	-	-	0.2	dB	
			I/Q phase mismatch	-5	-	5	Deg.	
			Data clock rate	-	-	13	MHz	
TXIOUTP	UEM	MJOELNER	Diff. Voltage swing	2.15	2.2	2.25	Vpp	Positive TX signal (program-able voltage swing)
			DC level	1.10	1.20	1.25	V	
			Source impedance	-	-	200	W	
			Data clock rate	-	-	13	MHz	
TXIOUTN	UEM	MJOELNER	Differential voltage swing	2.15	2.2	2.25	Vpp	Negative TX signal (program-able voltage swing)
			DC level	1.17	1.20	1.23	V	
			Source impedance	-	-	200	W	
			Data clock rate	-	-	13	MHz	
TXQOUTP	UEM	MJOELNER	Differential voltage swing	2.15	2.2	2.25	Vpp	Positive TX signal (program-able voltage swing)
			DC level	1.17	1.20	1.23	V	
			Source impedance	-	-	200	W	
			Data clock rate	-	-	13	MHz	
TXQOUTN	UEM	MJOELNER	Differential voltage swing	2.15	2.2	2.25	Vpp	Negative TX signal (program-able voltage swing)
			DC level	1.17	1.20	1.23	V	
			Source impedance	-	-	200	W	
			Data clock rate	-	-	13	MHz	

GENIO (28:0)			General purpose I/O					
GENIO5 (TXP)	UPP	MJOEL-NER	Logic "1"	1.38	-	1.80	V	Transmitter power control enable
			Logic "0"	0	-	0.4	V	
GENIO6 (RESETX_MJOEL)	UPP	MJOEL-NER	Logic "1"	1.38	-	1.80	V	Reset to RF chip
			Logic "0"	0	-	0.4	V	
RFAUXCONV(2:0)			RF / BB analogue control signals					
AUXOUT	UEM	MJOEL-NER	Output voltage	0.12	-	2.50	V	Transmitter power control
			Source imped-ance	-	-	200	W	
			Resolution	-	10	-	Bits	
Regulators			RF regulators					
VBAT (VBATREGS)	Bat-tery	PA / UEM	Output voltage	2.9	3.6	4.2	V	Battery cut-off is set by UEM to 2.9 V
VR2	UEM	MJOEL-NER	Output voltage	2.64	2.78	2.86	V	Supply to : TX – chain, Power Loop Control and Digital logic
			Current	0.1	-	100	mA	
VR3	UEM	MJOEL-NER	Output voltage	2.64	2.78	2.86	V	Supply to : Ref. Osc.
			Current	0.1	-	20	mA	
VR5	UEM	MJOEL-NER	Output voltage	2.64	2.78	2.86	V	Supply to : PLL, Divider, LO buffers
			Current	0.1	-	50	mA	
VR6	UEM	MJOEL-NER	Output voltage	2.64	2.78	2.86	V	Supply to : LNA's, Pregain
			Current	0.1	-	50	mA	
VR7	UEM	VCO	Output voltage	2.64	2.78	2.86	V	Supply to : LO buffers, Local oscillators
			Current	0.1	-	45	mA	
VREFRF01	UEM	MJOEL-NER	Output voltage	1.334	1.35	1.366	V	Used in MJOELNER (VBEXT) as 1.35V reference
			Current	-	-	100	µA	
			Current	-	-	100	µA	
VIO	UEM	MJOEL-NER	Output voltage	1.71	1.8	1.88	V	Supply to : BB buffer
			Current	0.1	-	150	mA	

Table 13: Board clocks

Signal name	From	To	Min	Typ	Max	Unit	Notes
RFCLK	MJOELNER	UPP	-	26	-	MHz	

Table 13: Board clocks

Signal name	From	To	Min	Typ	Max	Unit	Notes
SLEEPCLK	UEM	UPP	-	32.768	-	kHz	
RFCONVCLK	UPP	UEM		13	-	MHz	Active when RF converters are active
RFBUSCLK	UPP	MJOELNER	-	13	13	MHz	Only active when bus-enable is active
DBUSCLK	UPP (DSP)	UEM	-	13	13	MHz	Only active when bus-enable is active
CBUSCLK	UPP (MCU)	UEM	-	1	1	MHz	Only active when bus-enable is active
LCDCAMCLK	UPP	LCD	0.3	3.25 0.650	4	MHz	Only active when bus-enable is active

External Signals and Connections

System connector (X102)

Table 14: DC connector

Pin	Signal	Min	Nom	Max	Condition	Note
2	VCHAR	-	11.1V_{peak}	16.9 V_{peak} 7.9 V_{RMS} 1.0 A_{peak}	Standard charger (ACP-7)	Charger positive input
		7.0 V_{RMS}	8.4 V_{RMS}	9.2 V_{RMS} 850 mA	Fast charger	
1	CHGND	-	0	-		Charger ground

Table 15: External microphone

Signal	Min	Nom	Max	Condition	Note
MIC2P (Differential input P)	-	-	100mV_{pp}	G=20dB	1kΩ to MIC1B
MIC2N (Differential input N)	-	-	100mV_{pp}	G=20dB	1kΩ to GND
MIC2B (Microphone Bias)	2.0 V	2.1 V	2.25 V	DC	Unloaded
External loading of MICB2	-	-	600 uA	DC	

Table 16: External speaker, differential output XEARP(HF) & XEARN (HFCM)

Signal	Min	Nom	Max	Units	Note
Output voltage swing* ** seen from transducer side*	2.0	-	-	Vpp	Differential output, with 60 dB signal to total distortion ratio

Signal	Min	Nom	Max	Units	Note
Common voltage level for HF output (HF & HFCM) VCMHF	0.75	0.8	0.85	V	
Load resistance (HF to HFCM)	30	-	-	W	
Load capacitance (HF to HFCM)	-	-	10	nF	

Table 17: Headset detection

Signal	Min	Nom	Max	Condition	Note
HookInt	0 V	-	2.86 V (VANA)		Headset button call control, connected to UEMAD-converter
HeadInt	0 V	-	2.86 V (VANA)		Accessory detection, connected to UEMAD-converter

DC-OUT (J307,J308 and J309)

Table 18: DC-OUT Connections

Pad	Name	Parameter	Min	Typ	Max	Unit	Notes
J307	Power	Voltage (open)	-	-	Vbat	V	Output power line
		Current (short)	56	64	72	mA	
J308	CTI (Input)	Resistor value	30.9	-	750	kΩ	Cover detection
J309	GND	-	-	-	-	-	Ground

SIM (X387)

Table 19: SIM Connector

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
1	CLK	Frequency	-	3.25	-	MHz	SIM clock
		Trise/Tfall	-	-	50	ns	
2	RST	1.8V SIM Card	1.62 0	"1" "0"	VSIM 0.27	V	SIM reset (output)
		3V SIM Card	2.7 0	"1" "0"	VSIM 0.45	V	
3	VCC	1.8V SIM Card	1.6	1.8	2.0	V	Supply voltage
		3V SIM Card	2.8	3.0	3.2	V	
4	GND	GND	-	0	-	V	Ground
5	VCC		-	-	-		Not connected
6	I/O	1.8V Voh 1.8V Vol	1.62 0	"1" "0"	VSIM 0.27	V	SIM data (output)
		3 Voh 3 Vol	2.7 0	"1" "0"	VSIM 0.45	V	
		1.8V Vih 1.8V Vil	1.26 0	"1" "0"	VSIM 0.27	V	SIM data (input) Trise/Tfall max 1us
		3V Vil 3V Vil	2.1 0	"1" "0"	VSIM 0.45	V	

Functional Description

Modes of Operation

The NPM-8 baseband engine has five operating modes (in normal mode):

- Power_off
- Acting Dead
- Active
- Sleep
- Charging

Additionally, two modes exist for product verification: testmode and local mode.

Power_off

In this state, the phone is powered off, but supplied. VRTC regulator is active (enabled), having supply voltage from the main battery. Note, the RTC status in PWR_OFF mode depends on whether RTC was enabled or not when entering PWR_OFF. From Power_off mode, UEM enters RESET mode (after a 20 ms delay), if any of following statements is

true (logical OR –function):

- Power_on button detected (PWROFFX)
- Charger connection detected (VCHARDET)
- RTC_ALARM detected

The phone enters POWER_OFF mode from all the other modes except NO_SUPPLY if the internal watchdog elapses.

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called Acting Dead. In this mode, no RF parts are powered. To the user, the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge to the user that the battery is being charged.

Active

In the active mode, the phone is in normal operation — scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode, depending on whether the phone is in burst reception, burst transmission, the DSP is working, and so on.

In active mode, the RF regulators are controlled by the SW writing into UEM's registers wanted settings: VR1A/B must be kept disabled. VR2 can be enabled or forced into low quiescent current mode. VR3 is always enabled in active mode. VR4 -VR7 can be enabled, disabled, or forced into low quiescent current mode.

Table 20: Regulator controls

Regulator	Notes
VFLASH1	Enabled; low Iq mode during sleep
VFLASH2	Not used in NPM-8, must be kept disabled
VANA	Enabled; disabled in sleep mode
VIO	Enabled; low Iq mode during sleep
VCORE	Enabled; low Iq mode during sleep
VSIM	Controlled by register writing
VR1A	Not used in NPM-8, must be kept disabled
VR1B	Not used in NPM-8, must be kept disabled
VR2	Controlled by register writing; enabled in sleep mode
VR3	Enabled; disabled in sleep mode
VR4	Not used in NPM-8; must be kept disabled
VR5	Enabled; disabled in sleep mode
VR6	Enabled; disabled in sleep mode

Table 20: Regulator controls

Regulator	Notes
VR7	Enabled; disabled in sleep mode
IPA1-2	Not used in NPM-8, must be kept disabled

Sleep mode

Sleep mode is entered when both the MCU and DSP are in stand-by mode. Sleep is controlled by both processors. When SLEEPX low signal is detected, the UEM enters SLEEP mode. VCORE, VIO, and VFLASH1 regulators are put into low quiescent current mode. All RF regulators, except VR2, are disabled in SLEEP. When SLEEPX=1 is detected, the UEM enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt, generated by a charger connection, key press, headset connection, etc.

In sleep mode, the main oscillator (26MHz) is shut down and the 32 kHz sleep clock oscillator is used as reference clock for the baseband.

Charging

Charging can be performed in parallel with any other operating mode. A BSI resistor inside the battery pack indicates the battery type/size. The resistor value corresponds to a specific battery capacity and technology.

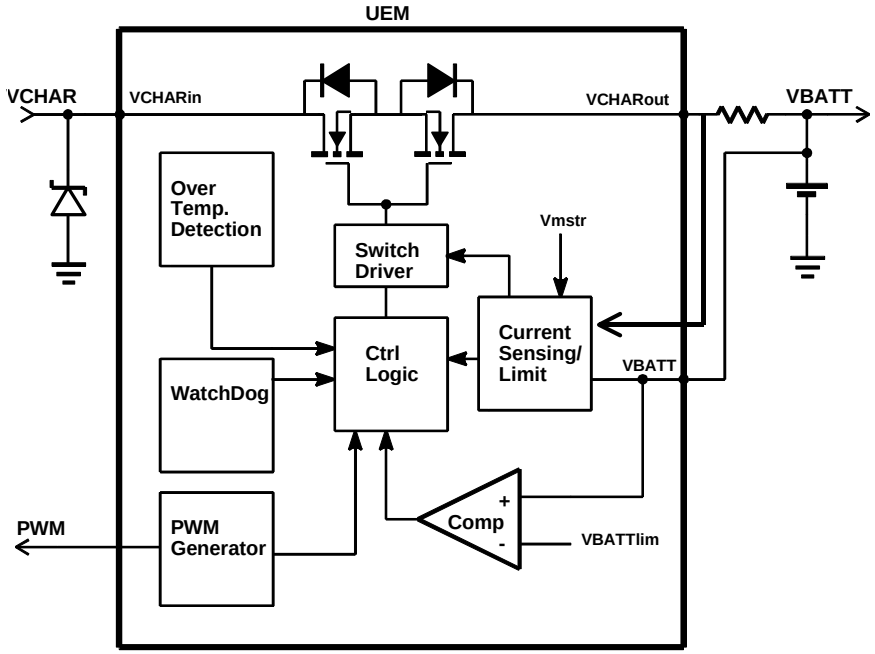
The battery voltage, temperature, size, and current are measured by the UEM, controlled by the charging software running in the UPP.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery. The battery voltage rise is limited by turning the UEM switch off when the battery voltage has reached VBATLim (programmable charging cut-off limits 3.6V / 5.0V / 5.25V). Charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Charging is controlled by the UEM ASIC. The external components are mounted for EMC, reverse polarity and transient protection of the input to the baseband module. The charger connection is through the system connector interface. Both 2- and 3-wire type chargers are supported.

The operation of the charging circuit has been specified in such a way as to limit the power dissipation across the charge switch and to ensure safe operation in all modes.

Figure 2: UEM charging circuitry



Charger Detection

Connecting a charger creates voltage on VCHAR input of the UEM. When VCHAR input voltage level is detected to rise above VCH_{DET+} threshold by UEM charging starts. VCHARDET signal is generated to indicate the presence of the charger for the SW.

The charger identification/acceptance is controlled by EM SW.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1 Check that the charger output (voltage and current) is within safety limits.

2 Identify the charger.

3 Check that the charger is within the charger window.

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

Charge Control

In active mode, charging is controlled by the digital portion of the UEM. Charging voltage and current monitoring is used to limit charge into a safe area. For that reason, UEM has programmable charging cut-off limits $VBATLim_{1,2L,2H}$ (3.6 V / 5.0 V / 5.25 V). Maximum charging current is limited to 1.2 A. Default for VBATLim is 3.6 V (used for initial charging of empty battery).

$VBATLim_{1,2L,2H}$ are designed with hysteresis. When the voltage rises above $VBATLim_{1,2L,2H}$+ charging is stopped by turning charging switch OFF. No change in oper-

ational mode occurs. After voltage has decreased below VBATLim_ charging restarts.

If VBAT is detected to rise above the programmed limit, the output signal OVV is set to '1' by CHACON. If charging current limit is reached, OVC output is set '1' by CHACON.

Pulse-width-Modulated (PWM) control signals PWM1 and PWM32 are generated by the digital portion of the UEM to CHACON block.

In principle, there are two PWM frequencies in use — depending on the type of the charger (standard charger 1 Hz, fast charger 32 Hz. Duty cycle range is 0% to 100%), but in NPM-8, only the 1 Hz mode will be used, as all charger will be treated as standard charges (2-wire types).

Supported Chargers

Supported chargers are:

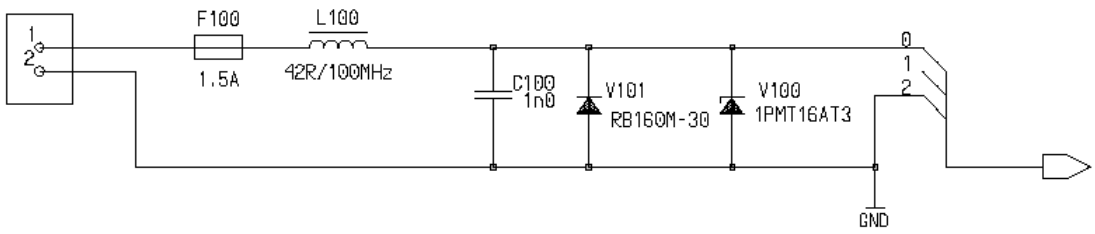
- 2-wire chargers: ACP-7, ACP-8, and ACP-12.
- 3-wire chargers: PPH-1, ACP-9, ACT-1, LCH-8, and LCH-9.

The 3-wire chargers have a 3-wire interface to the phone (2 power and 1 control). The control wire carries the 32 Hz digital pulse width modulated signal, which must be generated by the phone to control the charger output voltage. In NPM-8, the 32Hz PWM for the charger is connected to GND inside the bottom connector. This sets full charger output voltage and equals 0% PWM from charger point of view.

Charger Interface Protection

In order to ensure safe operation with all chargers and in misuse/fail situations, the charger interface is protected using transient voltage suppressor (TVS) and 1.5 A fuse. TVS used in NPM-8 is 16 V@175 W device. A Schottky diode is present to protect the charger input from reverse polarity chargers.

Figure 3: Charger interface



TVS characteristics:

Breakdown voltage (V_{BR})	17.8 Vmin (at I_T 1.0mA)
Reverse standoff voltage (V_R)	16 V
Max reverse leakage current at V_R (I_R)	5 uA
Max peak impulse current (I_{pp})	7 A (at Ta=25^o C, current waveform: 10/1000us)

Max clamping voltage at I_{pp} (V_c) 26 V

Charging Circuitry Electrical Characteristics

Table 21: Electrical Characteristics

Parameter Test conditions	Symbol	Min	Typ	Max	Units
Input voltage range (fast charger, no load)	VCHAR	7.0	8.4	9.2	V_{RMS}
Input voltage range (std charger, no load)		-	11.1 7.9	16.9	V_{peak} V_{RMS}
Absolute Maximum VCHAR voltage		-0.3	-	+20	V
Input resistance from VCharIn to ground	Rin	2	4	6	kΩ
Master reset threshold level	V_{MSTR+} VMSTR-	2.0 1.8	2.1 1.9	2.2 2.0	V
VCOFFX threshold levels	V_{COFF+} VCOFF-	3.0 2.7	3.1 2.8	3.2 2.9	V
VCHAR detection threshold level	VCH_{DET+} VCHDET-	1.9 1.7	2.0 1.8	2.1 1.9	V
Continuous input current (fast charger)	I_{CH}	-	-	850	mA
Maximum input current (std charger)	I_{CH}	-	-	1.0	A_{peak}
Start-up mode charging current	I_{START}	100	-	150	mA
PWM mode charge current	I_{LIM}	1.1	1.2	1.45	A
Output voltage (Battery voltage)	VBAT	0	3.6	4.2	V
Charging cut-off limits (programmable)	$VBATLim_{1+}$ VBATLim1- VBATLim2L+ VBATLim2L- VBATLim2H+ VBATLim2H-	3.54 3.32 4.85 4.65 5.10 4.90	3.65 3.50 5.0 4.85 5.25 5.10	3.76 3.66 5.15 5.05 5.40 5.30	V
Charging switch resistance (includes bonding and leads) Temp =65°C (ambient)	R_{SW}	-	-	0.3	W
PWM frequency (std charger)		0.5	1	1.5	Hz
PWM duty cycle		0	-	100	%
Switch output current slew rate	SR	0.4	0.6	0.8	A/ms
Charging thermal shutdown threshold	TjsdC+ TjsdC-	140 120	150 130	160 140	°C
VFLASH1 supply voltage input	VFLASH1	2.7	2.78	2.88	V

Note: VCHAR is used as a supply voltage for charging control parts.

Power Up and Reset

Power up and reset is controlled by the UEM ASIC. The NPM-8 baseband can be powered up in following ways:

1 Press power button, which means grounding the PWRONX pin of the UEM

2 Connect the charger to the charger input

3 Supply battery voltage to the battery pin

4 RTC Alarm, the RTC has been programmed to give an alarm

After receiving one of the above signals, the UEM counts a 20 ms delay and then enters its reset mode. The watchdog starts up and, if the battery voltage is greater than Vcoff+, a 200 ms delay is initiated to allow references, etc., to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500 us later, VR3, VANA, VIO, and VCORE are enabled. Finally, the PURX line is held low for 20 ms. This reset, PURX, is fed to the baseband ASIC UPP; resets are generated for the DSP and the MCU. During this reset phase, the UEM forces the VCXO regulator on, regardless of the status of the sleep control input signal to the UEM. All baseband regulators are switched on at the UEM power on, except for the SIM regulator that is controlled by the MCU. The UEM internal watchdog is running during the UEM reset state, with the longest watchdog time selected. If the watchdog expires, the UEM returns to power off state. The UEM watchdog is internally acknowledged at the rising edge of the PURX signal in order to always give the same watchdog response time to the MCU.

Power up with PWR key

When the power on key is pressed, the UEM enters the power up sequence as described in the *Power Up and Reset s*ection. Pressing the power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEM. This means that when the power key is pressed, an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEM interrupt register and notices that it is a PWRONX interrupt. The MCU now reads the status of the PWRONX signal using the UEM control bus, CBUS. If the PWRONX signal stays low for a specified time, the MCU accepts this as a valid power on state and continues with the SW initialization of the baseband. If the power on key does not indicate a valid power on situation, the MCU powers off the baseband.

Power up when charger is connected

In order to be able to detect and start charging in a case where the main battery is fully discharged (empty) and hence UEM has no supply (NO_SUPPLY mode of UEM), charging is controlled by *START-UP CHARGING* circuitry.

Whenever VBAT level is detected to be below master reset threshold (V_{MSTR-}), charging is controlled by START_UP charge circuitry. Connecting a charger forces VCHAR input to rise above charger detection threshold, VCH_{DET+}. By detection start-up charging is started. UEM generates 100mA constant output current from the connected charger's output voltage. As the battery charges, its voltage rises, and when the VBAT voltage level

is higher than the master reset threshold limit (V_{MSTR+}) is detected and the START_UP charge is terminated.

The charge control block (CHACON) monitors the VBAT voltage level. MSTRX='1' output reset signal (internal to UEM) is given to UEM's RESET block when VBAT>V_{MSTR+} and the UEM enters into a reset sequence described in the *Power Up and Reset* section.

If VBAT is detected to fall below V_{MSTR-} during start-up charging, charging is cancelled. It will restart if new rising edge on VCHAR input is detected (VCHAR rising above VCH_{DET+}).

Power up when battery is connected

Baseband can be powered up by connecting a battery with sufficient voltage. Battery voltage has to be higher than the UEM internal comparator threshold level, V_{coff+}. When battery proper voltage is detected, the UEM enters the reset sequence as described in the *Power Up and Reset* section. This power up sequence is meant for test purposes; in normal use (Btemp resistor > 1kΩ) the phone will power off again immediately, without noticing the user.

RTC alarm power up

If the phone is in POWER_OFF mode when RTC alarm occurs, the wake up procedure is as described in the *Power Up and Reset* section. After the baseband is powered on, an interrupt is given to MCU. When the RTC alarm occurs during ACTIVE mode, the interrupt for MCU is generated.

A/D Channels

The UEM contains the following A/D converter channels that are used for several measurement purposes. The general slow A/D converter is a 10-bit converter using the UEM interface clock for the conversion. An interrupt will be given at the end of the measurement.

The UEM's 11-channel analog-to-digital converter is used to monitor charging functions, battery functions, voltage levels in external accessory detection inputs, user interface, and RF functions.

When the conversion begins, the converter input is selected. Then the signal processing block creates a data with MSB set to '1' and others to '0'. In the D/A converter, this data controls the switches, which connect the input reference voltage (VrefADC) to the resistor network. The generated output voltage is compared with the input voltage under measurement and if the latter is greater, MSB remains '1' else it is set '0'. The following step is used to test the next bit and the next, until LSB is reached. The result is then stored to the ADCR register for the UPP to read.

The monitored battery functions are battery voltage (VBATADC), battery type (BSI), and battery temperature (BTEMP) indication.

The battery type is recognized through a resistive voltage divider. In the phone there is a

100 kOhm pull up resistor in the BSI line and the battery has a pull-down resistor in the same line. Depending on the battery type, the pull-down resistor value is changed. The battery temperature is measured equivalently, except that the battery has a NTC pull-down resistor in the BTEMP line.

KEYB1&2 inputs are made for keyboard scanning purposes. These inputs are also routed internally to the miscellaneous block. KEYB1&2 inputs are not used In NPM-8, and the connected interrupts must be kept disabled by the SW.

The HEADINT and HOOKINT are external accessory detection inputs used for monitoring voltage levels in these inputs. They are routed internally from the miscellanous block and they are connected to the converter through a 2:1 multiplexer.

PATEMP and VCXOTEMP channels are not used as originally intended. PATEMP input is used for the detection of accessory covers (CTI). VCXOTEMP is not used in NPM-8.

Table 22: Slow A/D converter characteristics

Characteristics	Min	Typ	Max	Unit
Number of bits	10			bits
Integral nonlinearity	-	-	+/- 2	LSB
Differential nonlinearity	-	-	+/- 2.5	LSB
Conversion time	-	-	11	µs
Input voltage range (1)	0	-	2.7	V
Input capacitance	4	5	6	pF

(1) *AD converter is calibrated in production.*

Table 23: Slow A/D converter input ranges

Signal	Min	Typ	Max	Unit	Notes
VBATADC	2.7	-	5.25	V	Physical input on UEM is VBATREGS
ICHAR	VBATADC	-	VBATADC+0.316	V	
VCHARADC	0.1	-	1.35	V	
BSI	0	-	2.7	V	
BTEMP	0	-	2.7	V	
PATEMP	0	-	2.7	V	Used for CTI
VCXOTEMP	0	-	2.7	V	Not used in NPM-8
HEADINT	0	-	2.7	V	
HOOKINT	0	-	2.7	V	
LS	0	-	2.7	V	Not used in NPM-8
KEYB1	0	-	2.7	V	Not used in NPM-8

(1) AD converter is calibrated in production.

Table 23: Slow A/D converter input ranges

Signal	Min	Typ	Max	Unit	Notes
KEYB2	0	-	2.7	V	Not used in NPM-8

AD converter is calibrated in production.

Battery Voltage Measurement A/D Channel (VBATADC)

The battery voltage is scaled inside the UEM in order to avoid external components. The maximum battery voltage that gives a full A/D reading is 5.25 V.

Battery voltage can be connected to sample-and-hold circuit either through a resistive voltage divider or through a voltage-scaling circuit. The voltage-scaling circuit is used to get larger input voltage range for the converter than what is achieved with the resistive divider. The sample-and-hold circuit is used to measure the battery voltage during transmit burst. Otherwise, the S/H circuit is bypassed. Note that both the battery voltage (VBATADC) and the charger voltage (VCHARADC) are sampled whenever the sampling function is used.

Charger Voltage Measurement A/D Channel (VCHARADC)

This channel is used to measure the charger input voltage VCHAR. The charger input idle voltage is measured to identify the charger. Associated with the charger voltage measurement, an envelope detector is used to detect a rectifier bridge type of charger. Connection of the charger is performed by the rising edge of the charger input. The charger must be a full-wave rectifier. A half-wave rectifier charger has to be rejected.

This A/D channel has a built-in feature built that allows the charger voltage measurement to be specified to be performed whether the charger switch is closed or open. This information is provided by the MCU when this channel is addressed.

The charger measurement A/D channel can also be timed to the charger envelop detector in order to measure the standard charger peak voltage.

Charger Current Measurement A/D Channel (ICHAR)

This A/D channel is used to measure the charger current ICHAR. The current sensor is implemented using a 0.22Ω resistor in series between the UEM charging voltage output and the battery voltage. The voltage drop over the resistor is examined. The charger current measurement is used for charger detection and maintenance charging PWM calculations.

Battery Temperature Measurement A/D Channel (BTEMP)

The temperature of the battery pack is monitored during charging. The battery pack is equipped with an NTC resistor (value is 47 kOhm at 25^{o} C). The BTEMP signal is connected on the baseband to the UEM. An external 100 kOhm pull-up is needed.

Battery Size Measurement A/D Channel (BSI)

This channel is used to identify the battery. The battery pack BLC-2 has a resistor 75kOhm connected to ground. An external 100kOhm pull-up resistor is on the phone side. The BSI signal is connected to the UEM.

External Accessory Detection A/D Channel (HEADINT, HOOKINT)

An A/D converter channel is used to detect DCT4-type accessories. An A/D converter channel is used to measure the DC level on the external microphone. The detection is implemented using a pull-down resistor in the accessory and a pull-up on the baseband side. The pull-up resistor on the baseband side is internal to the UEM. This A/D channel is internally connected to either HeadInt or HookInt.

PA Temperature measurement A/D Channel (PATEMP)

In NPM-8, this A/D channel is used for Cover Type Detection (CTI) in conjunction with DC-OUT covers. The detection is implemented using a pull-down resistor in the accessory and a pull-up on the baseband side.

LCD & Keyboard Backlight

LCD Backlight

The LCD Backlight consists of two TBSF (Through the Board Side Firing) yellow/green LEDs, which are placed on the main PWB below the LCD area. They light into the light guide where the light is distributed to generate sufficient backlight for the LCD.

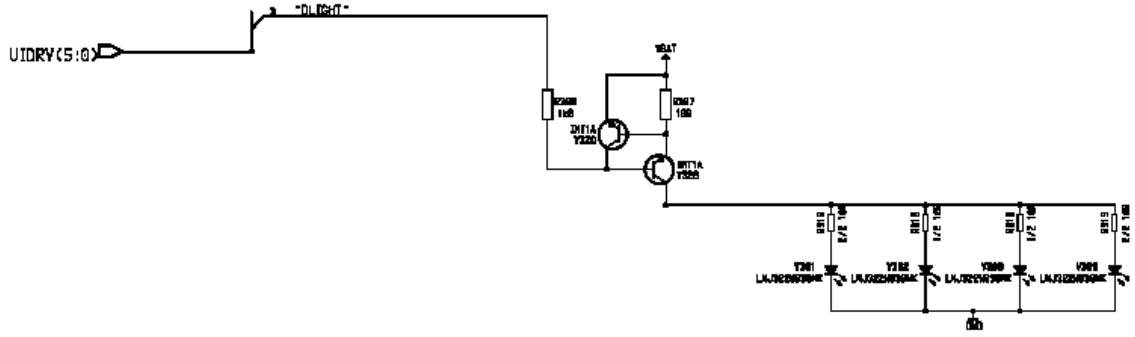
Keyboard light

The keyboard light consists of two TBSF yellow/green LEDs, which are placed under the keyboard and use the light guide to distribute the light.

LED driver circuit

The LED drivers for the LCD & Keyboard backlight are shared as shown in the following figure. The driver circuit is controlled by the UEM output pin [DLIGHT] and drive current is 15 mA per LED. By using appropriate SW, the driver can be PWM-controlled for dimming purposes.

Figure 4: Shared LED driver circuit for LCD and Keyboard backlight



LCD cell

The LCD is a black-and-white 96x65 full dot matrix display. The LCD has a standard DCT4

interface. The LCD interface between the LCD cell and the main PWB can be viewed in the *LCD* section. The LCD cell is part of the complete LCD module, which includes metal frame, gasket, light guide, spring connector, transflector, dome sheet, and earpiece.

The LCD is powered from both V_{FLASH1} and V_{IO}. V_{FLASH1} is used for the boosting circuit and V_{IO} for the driver chip.

SIM Interface

The UEM contains the SIM interface logic level shifting. The SIM supports 3 V and 1.8 V SIMs. SIM supply voltage is selected by a register in the UEM. It is only allowed to change the SIM supply voltage when the SIM IF is initialized.

The SIM power up/down sequence is generated in the UEM. This means that the UEM generates the RST signal to the SIM. Also the SIMCardDet signal is connected to the UEM. The card detection is taken from the BSI signal, which detects the removal of the battery. The monitoring of the BSI signal is done by a comparator inside the UEM. The comparator offset is such that the comparator output does not alter the state as long as the battery is connected. The threshold voltage is calculated from the battery size specifications.

The SIM interface is powered up when the SIMCardDet signal indicates "card in". This signal is derived from the BSI signal.

Table 24: BSI Detection

Parameter	Variable	Min	Typ	Max	Unit
BSI comparator threshold	Vkey	1.94	2.1	2.26	V
BSI comparator hysteresis (1)	Vsimhyst	50	75	100	mV

(1) Hysteresis is defined as [Vkey(+)-Vkey(-)] / 2

The SIM interface is located in the two ASICs: UPP and UEM.

The SIM interface in the UEM contains power up/down, port gating, card detect, data receiving, ATR-counter, registers, and level-shifting buffers logic. The SIM interface is the electrical interface between the Subscriber Identity Module Card (SIM Card) and mobile phone (via the UEM device).

The data communication between the card and the phone is asynchronous half-duplex. The clock supplied to the card is 3.25MHz. The data baud rate is SIM card clock frequency divided by 372 (by default), 64, 32, or 16. The protocol type that is supported is T=0 (asynchronous half-duplex character transmission as defined in ISO 7816-3).

The internal clock frequency from the UPP CTSI block is 13MHz in GSM. To achieve the minimum starting SIMCardClk rate of 3.25 MHz (as is required by the authentication procedure) and the duty cycle requirement of between 40% and 60%, the slowest possible clock supplied to the SIM has to be in the GSM system clock rate of 13/4MHz.

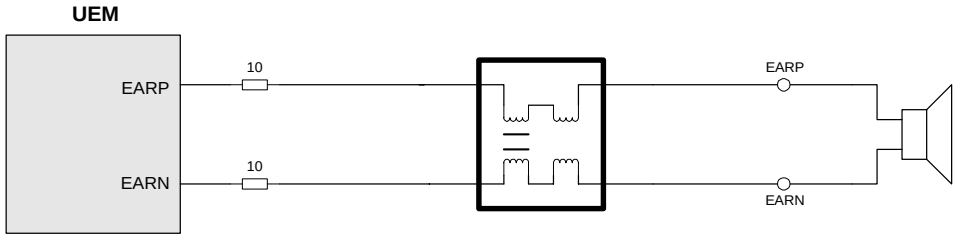
Internal Audio

Earpiece

The earpiece selected for NPM-8 is the standard DCT3 13-mm earpiece. The earpiece design is leak-tolerant.

The internal earpiece is a dynamic earpiece with an impedance of 32Ω. The earpiece is a low-impedance type, since the sound pressure is to be generated using current and not voltage (supply voltage is restricted to 2.7 V). The earpiece is driven directly by the UEM; the earpiece driver in the UEM is a bridge amplifier.

Figure 5: Speaker Interface



Internal Microphone

NPM-8 uses an omnidirectional microphone that is located in the system connector, sealed in a rubber gasket.

The microphone is biased from the UEM MICB1 output and lowpass filtered through an RC filter (470_,22uF) giving 20 dB attenuation at 217 Hz. The signal path from the microphone is lowpass filtered (2.2k_,1nF) and EMC decoupled (22pF)

The two 33nF capacitors are used to create a 1st order high-pass filter. The input impedance of the gain stage at MIC1P/N is the other part of the RC circuit. The high-pass filter is required due to low-frequency noise, which is one phenomenon identified as a problem when the internal microphone is used as handsfree microphone (PPH-1/carkit mode).

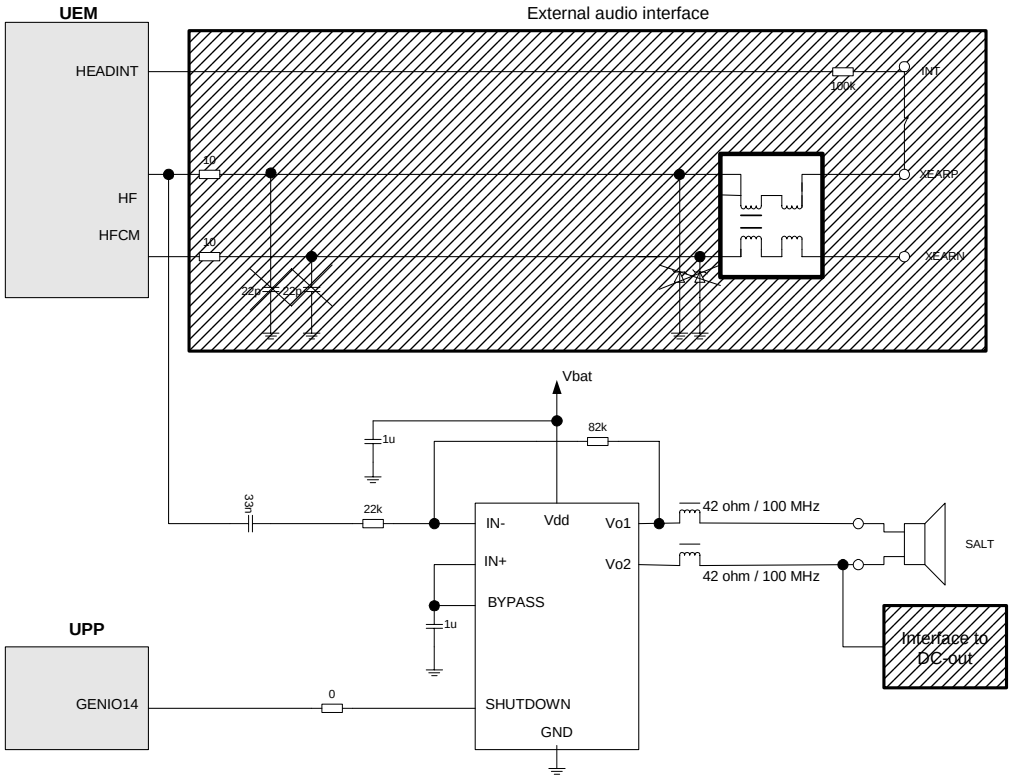
Ringer

A 13 mm speaker is used to generate alerting tones and melodies to indicate incoming calls, as well as used to generate game sound, keypress, and warning tones for the user.

Alerting tones and MIDI melodies are generated by the speaker, which is controlled by a sine driven output from the UEM and an external amplifier.

The speaker is electrically connected to the PWB by spring contacts (similar to that for the internal earpiece).

Figure 6: Ringer interface



Accessories

NPM-8 supports Li-ion and NiMH batteries, "footprint" "C" from the DCT4 Lion/Janette battery program.

Signal name	Pin number	Function
VBAT	1	Positive battery terminal
BSI	2	Battery capacity measurement (fixed resistor, connected to GND, inside the battery pack)
BTEMP	3	Battery temperature measurement (measured by ntc resistor connected to GND inside pack)
GND	4	Negative/common battery terminal

The BSI fixed resistor value indicates the type and default capacity of a battery; NTC resistor BTEMP measures the battery temperature.

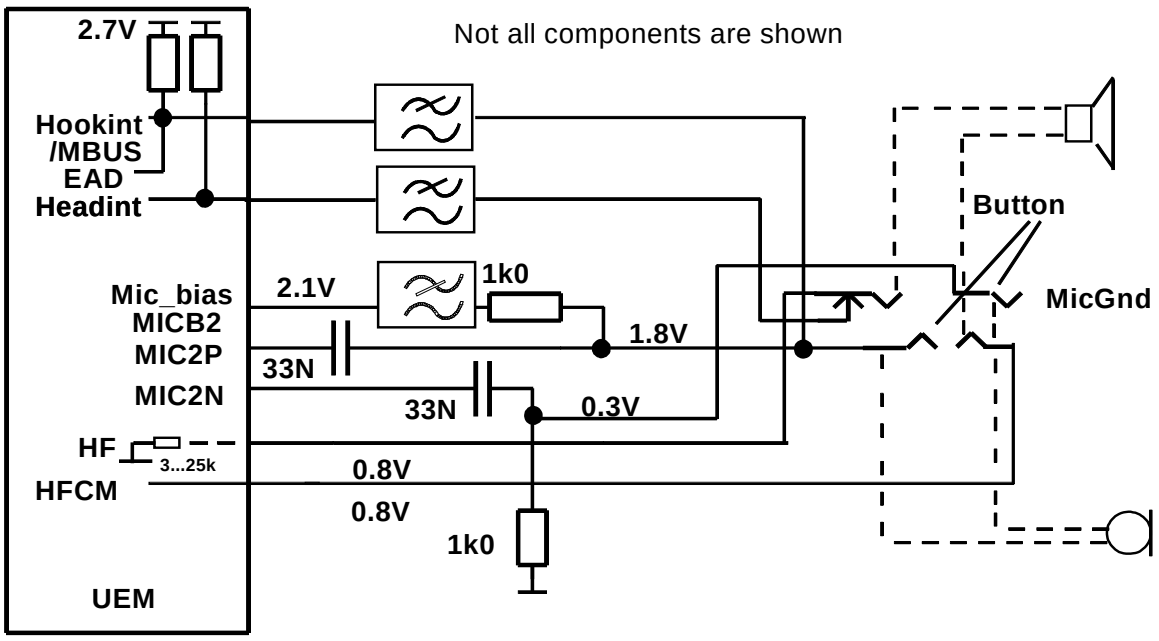
Temperature and capacity information are needed for charge control. These resistors are connected to the BSI and BTEMP pins of the battery connector. The P\phone has 100 kΩ pull-up resistors for these lines so that they can be read by A/D inputs in the phone.

External Audio

NPM-8 supports fully differential external audio accessory connection. A headset and PPH-1 can be directly connected to the system connector. Detection of the different

accessories is made in analog by reading the DC voltage value of the EAD converter.

Figure 7: Headset interface



Analog Audio Accessory Detection

The accessory is detected by the HeadInt signal when the plug is inserted. Normally when no plug is present, the internal pull-down on the HF pin pulls down the HeadInt signal. HeadInt comparator value is 1.9 V. When the plug is inserted, the switch in the connector is opened and the HeadInt signal is pulled up by the internal pull-up. The 1.9 V threshold level is reached and the comparator output changes to low state, causing an interrupt. The reverse is true when the accessory is disconnected: the HeadInt switch is closed and the HeadInt is pulled down.

Table 25: Truth table for HookInt and HeadInt

	HookInt	HeadInt
Basic Headset, fully differential	H	H
Button Headset (Switch closed)	L	H
Button Headset (Switch open)	H	H
PPH-1	H	H
No accessory	H	L

HeadInt signal is used to detect when the accessory is connected.

HookInt signal is used to detect when the button of the headset is pressed.

NOTE : Charging must be disabled during identification of PPH-1.

Headset Detection

Supported headsets are four-wire fully differential accessories. Detection of the headset can be split into five main phases:

1 Micbias is set to high impedance state

2 HeadInt interrupt is detected

3 EAD reading below 0.35V

4 Micbias is set active 2.1V

5 EAD reading 1.0V - 2.2V -> Headset connected

Table 26: Headset identification

Name	Function	Min	Typ	Max	Unit	Description
Headint	Accessory detection	2.2	2.78	2.86	V	Accessory connected
Ead / hookint	Micbias=High-Z			0.35	V	Headset
	Micbias active 2.1V	1.009	1.07	1.163	V	Headset button closed
		1.596	1.85	2.140	V	Headset button open

The hook signal is generated by creating a short circuit between the headset microphone signals. When no accessory is present, the HookInt signal is pulled up by the UEM. When the accessory is inserted and the microphone path is biased, the HookInt signal decreases to 1.8 V due to the microphone bias current flowing through the upper bias resistor network. When the button is pressed, the microphone signals are connected together and the HookInt will fall below trigger threshold level (1.35 V). This change in DC level will cause the HookInt comparator output to change state.

HeadInt comparator reference level is 1.90 V, +/- 0.15 V. HookInt comparator reference is selected by SW. Used trigger level is 1.35 V, +/- 10 mV.

PPH-1 Detection

PPH-1 accessory uses a four-wire fully differential audio connection. The accessory is detected by the Headint signal when the plug is inserted. PPH-1 has two operating modes with internal and external microphone. These modes can be separated by reading the EAD value. Detection of the PPH-1 can be split into three main phases:

1 Micbias is set to high impedance state

2 HeadInt interrupt is detected

3 EAD reading is 2.0V - 2.7V -> PPH-1 connected

Table 27: PPH-1 identification

Name	Function	Min	Typ	Max	Unit	Description
HeadInt	Accessory detection	2.2	2.78	2.86	V	Accessory connected
Ead / HookInt	Micbias = High-Z	2.064	2.182	2.302	V	PPH-1 external mic
		2.487	2.603	2.720	V	PPH-1 internal mic
		1.840			V	PPH-1 speaker mute

The PPH-1 has a function of speaker mute. It can be muted by setting micbias in low state.

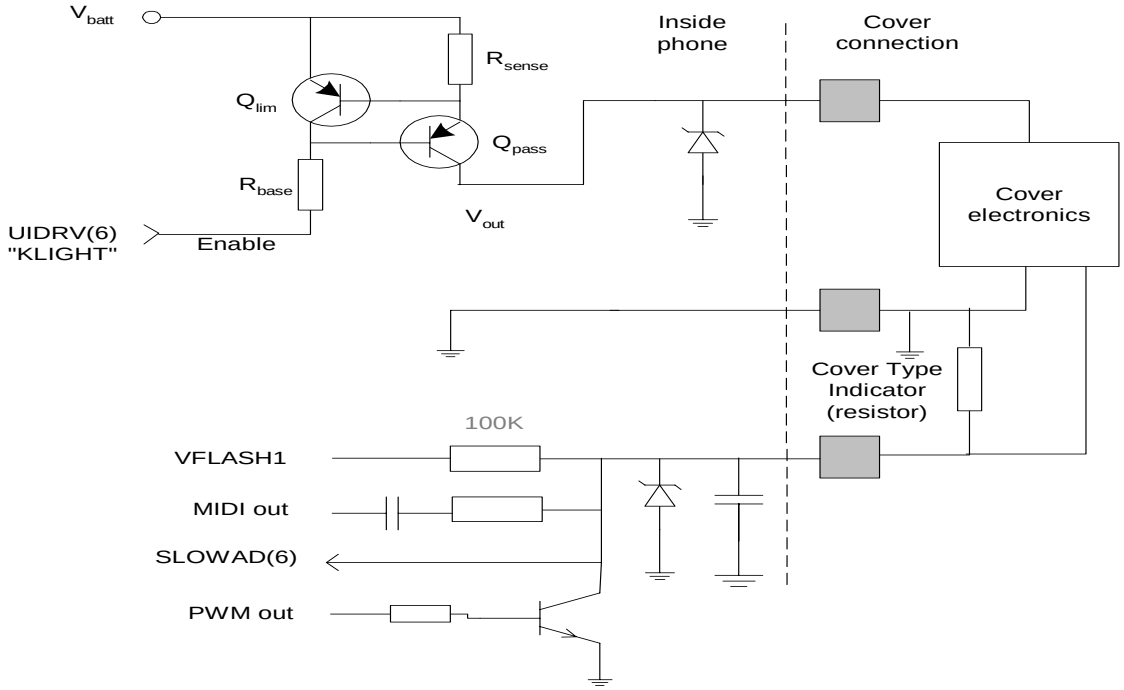
DC-OUT Interface

A special type of electrically A-cover called "DC-Out cover" is supported by the phone via an electrical/mechanical interface connection. The kind of circuit that has to be powered can be anything from simple LEDs to a "smarter" type of circuit.

Implementation

The implemented concept, which is using three pads/connections between the phone and the accessory cover, is shown in the figure below.

Figure 8: DC-OUT Interface



Detection of the cover is done via a "CTI" (Cover Type Indicator), which basically serves the same purpose as the BSI resistors in the battery packs. Detection will be done in the same way as currently used for the BSI. By using the "CTI", covers may be categorized into different groups (*i.e.*, current consumption).

The power section has a current-limited switch, and is controlled by a logic enable (on/off) via KLIGHT. On/off will be synchronised with the "VIBRA" signal SW wise, but can have independent SW control.

Keyboard

The keyboard used in NPM-8 is part matrix ("metal dome" type) and part individual interrupts. This is needed for supporting multiple key presses.

The keyboard PWB layout consists of a grounded outer ring and either a "cake pattern" grid (matrix) or an inner pad. This construction makes the keys immune for ESD, as the keydome will have a low ohmic contact with the PWB ground.

All lines are configured as input — when no key is pressed, the inputs are high since the UPP has internal pull-up resistors on those lines. When a key is pressed, the specific lines where the key is placed are pulled low. This generates an interrupt to the MCU and the MCU now starts its scanning procedure.

The matrix detection requires that two lines are pulled low at the same time. The matrix contains 15 keys. The six individual keys are detected by simple high-to-low transition interrupt.

When the key has been detected, all the keypad registers inside the UPP are reset and it's ready to receive a new interrupt.

RF Interface Block

The interface between the baseband and the RF can be divided into two categories:

1. The digital interface from the UPP to the RF ASICs (Mjoelner and Bifrost). The serial digital interface is used to control the operation of the different blocks in the RF ASICs.

2. The analog interface between the UEM and the RF. The analog interface consists of RX and TX converter signals. The power amplifier control signal TXC and the AFC signal also are from the UEM.

Memory Module

The NPM-8 baseband memory module consists of a 64-Mbit (8MB) external burst type flash memory and an 8-Mbit internal SRAM (the SRAM is part of the UPP and will not be covered here).

Memory Interface

The memory interface consists of the MEMADDA [23:0] address/data bus, the MEM-CONT[9:0] memory control bus, and the GENIO[23], which also is used for memory control.

The purpose of the memory interface is to reduce the amount of interconnections by multiplexing the address and the data signals on the same bus. Since the required flash address space is more than 16-bits, the MEMADDA[15:0] are multiplexed address/data

lines and MEMADDA[21:16] are only address lines, which in total allow for 4M addresses (MEMADDA[21:0]). The multiplexed data/address lines require the memory to store the address during the first cycle in the read/write access. Data access to the flash is performed as a 16-bit access (MEMADDA[15:0]) in order to improve the data rate on the bus.

The memory interface supports asynchronous read, burst mode synchronous read, and simultaneous read-while-write/erase, all controlled by the UPP.

Memory Description

The 64-Mbit density flash with 16-bit data access operates in both asynchronous random access and synchronous burst access (with crossing partition boundaries) and has various data protection features. Upon power up or reset, the device defaults to asynchronous read configuration. Synchronous burst read is indicated to the device by writing to the flash configuration register and can be terminated by deactivating the device.

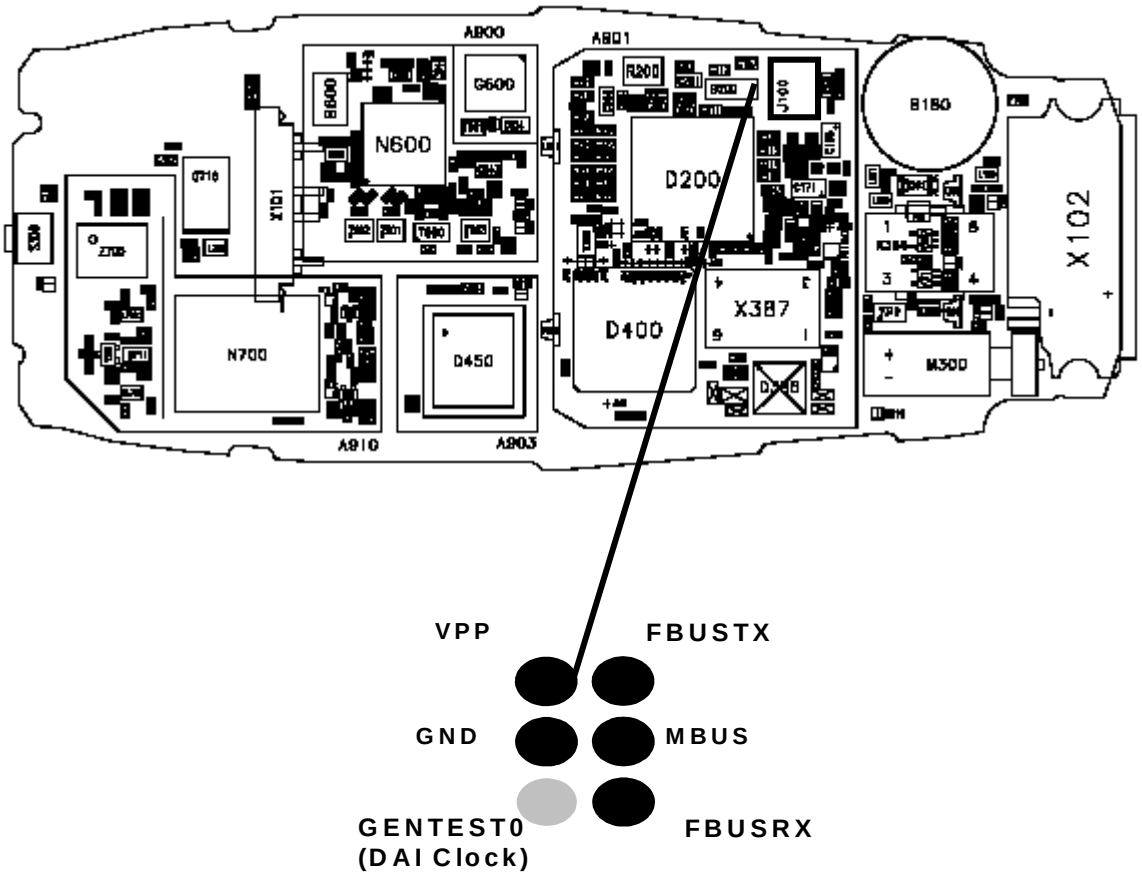
The device supports reads and in-system erase, and program operations at Vcc=1.8 V (Voltage range 1.7-1.9 V). Flashing at production is supported at Vpp=12 V (for limited exposure length only).

Test Interfaces

Through MBUS or FBUS connections, the phone HW can be tested through the Phoenix service sofware.

Service Interface

Figure 9: Production/Test/Customer Care interface



RF Module

This section describes the blocks of the RF engine, the RF requirements, and the environmental requirements for the NPM-8 RF engine.

Environmental specifications

Normal and extreme voltages

Nominal voltage:	3.6 V
Lower extreme voltage:	0.9 x 3.6 = 3.25 V
Higher extreme voltage:	5.15 V

Main technical specifications

Table 28: Nominal and maximum ratings

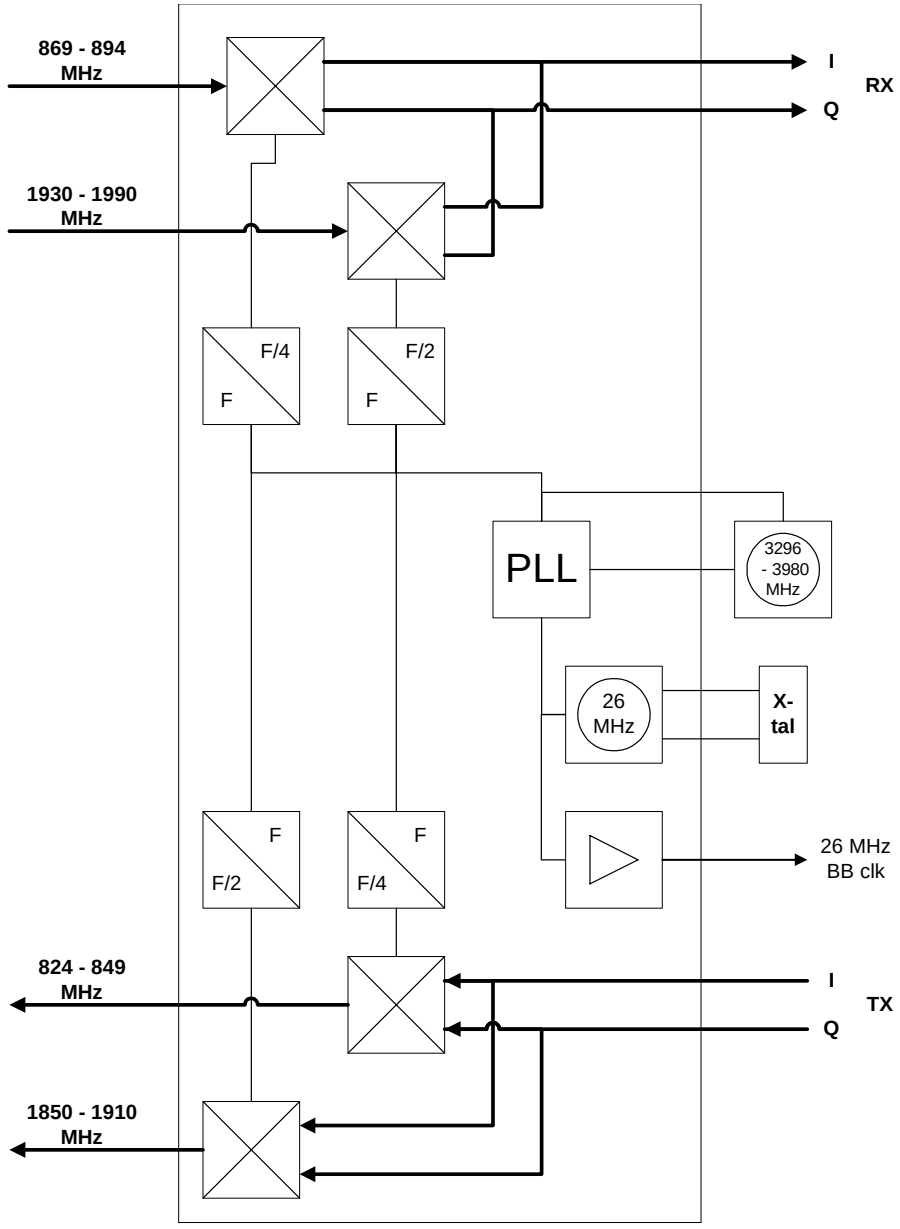
Parameter	Rating
Battery voltage - nominal	3.6 V
Battery voltage - maximum	5.2 V

Table 28: Nominal and maximum ratings

Parameter	Rating
Battery voltage - minimum	3.2 V
Regulated supply voltage - analog	2.78 V +/-3%
Regulated supply voltage - digital	1.8 V +/- 4.5%
Voltage reference	1.35 V +/-1.2%
Operating temperature range	
Normal operation	-10 ... +55^{o} C fulfilling GSM spec.
Reduced performance	(no damage): -30 +60^{o} C

RF frequency plan

Figure 10: RF Frequency plan



DC characteristics

Regulators

The transceiver has a multi-function power management IC (UEM) in the baseband section, which contains among other functions six 2.78 V regulators, a 1.8 V regulator, and two reference outputs.

All regulators can be controlled individually with 2.78 V logic directly or through control register.

Use of the regulators can be seen in the power distribution diagram. VrefRF01 is used as the reference voltages for the RX ADCs reference in Mjoelner.

The regulators are connected to Mjoelner, either directly or through output loading networks. The individual regulator can be switched on/off through the serial data bus in order to reduce the power consumption.

List of the needed supply voltages:

Voltage source	Load
VR1	Not used
VR2	Mjoelner, VTX (TX modulator)
VR3	Mjoelner, VXO (VCXO - digital logic)
VR4	Digital interface, Bifrost
VR5	Mjoelner, VPLL (Dividers - lo_buffers - PLL_charge - PLL_prescaler- PLL_counters)
VR6	Mjoelner, VRX (Front_end LNA- Pre_gain - BB section)
VR7	Bifrost, VVCO (VCO_buf VCO_core VCO_bias)
VrefRF01	Mjoelner, VREF1 (ref. Voltage)
VrefRF02	Not used
Vbatt	PA

Typical current consumption

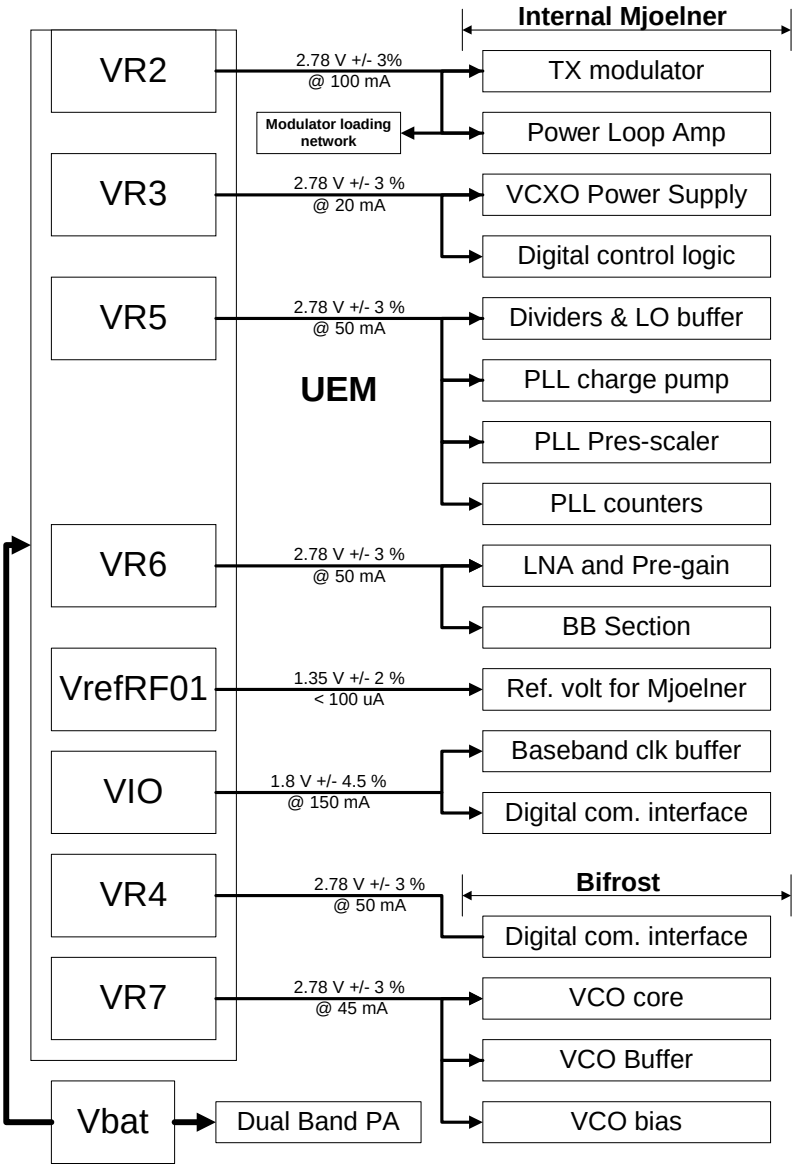
The table shows the typical current consumption in different operational modes.

Table 29: Current consumption information

Operation mode	Current consumption	Notes
Power Off	< 10uA	Leakage current (dual band PA)
Idle	1.2 mA	
RX	87.2 mA, peak	
TX, without PA	121 mA, peak	Not including TX buffer (max 10 mA)
TX, power level 5, GSM850	1700 mA, peak	Efficiency 48% (at max power – 1 dB)
TX, power level 0, GSM1900	1220 mA, peak	Efficiency 40% (at max power – 1 dB)

Power distribution diagram

Figure 11: Power Distribution



Frequency synthesizers

VCXO

The VCXO is an on-chip oscillator with off-chip crystal. The oscillator in itself is balanced with two independent outputs. One output is used inside the ASIC as reference for the PLL. The second output is for the baseband, an output that can be filtered inside the ASIC, controlled by SW. The reference for the BB is SW selectable to be either 13 MHz or 26 MHz. The reference frequency for NPM-8 will be 26 MHz in order to ease the suppression of the reference spurious.

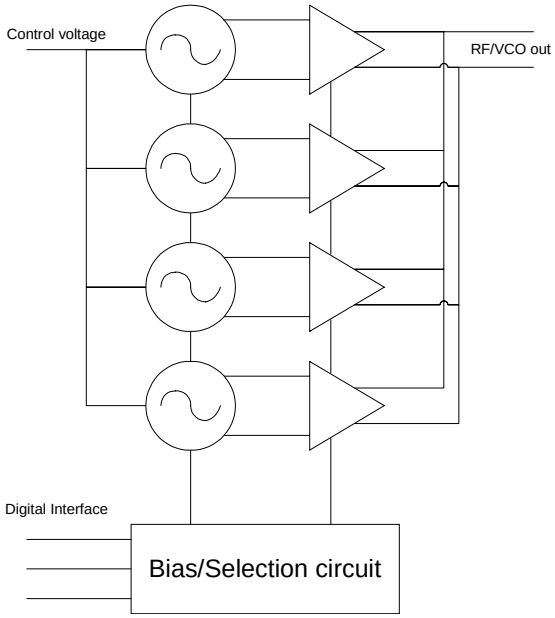
The drive level of the crystal can be adjusted by software control; the frequency accuracy is controlled by software with digital frequency inputs. The digital frequency control is divided between calibration and AFC.

VCO

The VCO is an ASIC with all the frequency determining parts inside. The VCO is balanced in order to decrease the influence of radiated distortion/noise from the surroundings, by common mode suppression, and to reduce the second harmonics relative to the fundamental frequency.

In order to reduce the requirements of the tuning voltage and coverage of the VCO, the VCO core is composed of four VCOs in parallel. This VCO circuit enables a very wide tuning range of 3.4 - 4.0 GHz with good phase noise performance. Each of the VCOs can be selected individually, but a digital section is also capable of automatically selecting the correct VCO, according to the programming of the PLL divider registers. This is accomplished as the digital control of the VCO decodes the setting of the dividers in Mjoelner and, based upon this, selects the correct VCO.

Figure 12: Block diagram of Bifrost



PLL Synthesizer, Functional Description

The frequency synthesis PLL, in conjunction with the VCO and 2/4 dividers, generates the LO signal for both RX and TX paths, locked to the VCXO (which itself is locked to the base station through the AFC).

Input to the PLL is the differential VCO and the 26 MHz reference oscillator signals. The VCO signal is divided by a swallow counter consisting of a 64/65 dual modulus divider and NDIV/ADIV dividers. The output of the NDIV/ADIV dividers is resynchronized in the phase detector with the output of the dual modulus divider to reduce phase noise.

The reference oscillator signal is divided by the RDIV divider to uptain a 400 kHz signal to be used as reference in the Phase detector. The output of this divider is also resynchronized in the phase detector with the reference input to reduce phase noise.

The divided signals are compared in a phase detector, which controls the charge pump.

The output of the charge pump is connected to the external loop filter.

The average output current of the charge pump is a linear function of the phase difference between the two input signals to the phase detector with a transfer constant of approximately 1 mA/2π. The transfer characteristic depends on which of the two available phase detectors is selected.

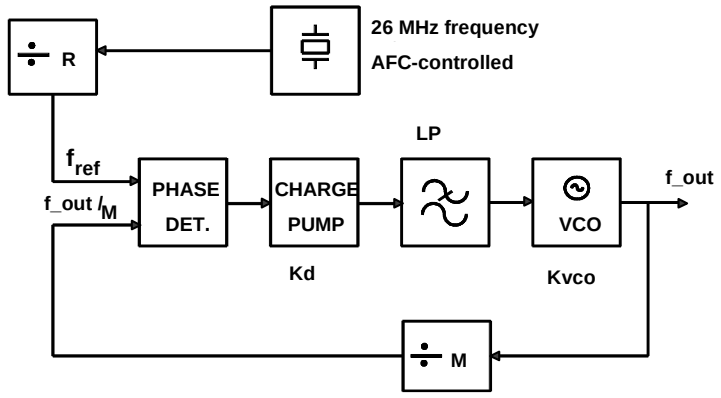
One detector is the linear phase detector where the current in the current sources of the charge pump is 1 mA independently of phase difference and a completely linear transfer characteristic is achieved.

The other phase detector is the piecewise linear phase detector where the current is reduced to 500 µA when sourcing and sinking current sources are active simultaneously. This results in a constant slope transfer characteristic with two discontinuities.

The loop filter averages the pulses from the phase detector and generates a DC control voltage to the VCO. The loop filter defines the step response of the PLL (settling time), affects the stability of the loop, and performs reference sideband rejection.

The following figure shows a simplified block diagram of the synthesizer.

Figure 13: Simplified Synthesizer



Receiver

The receiver is a dualband, direct-conversion, linear receiver. The received RF signal is routed from the antenna to the RX/TX switch. The RX/TX switch performs both the switching between receive – transmit routing of the antenna signals as well as the selection of the band to be used.

The RX signal is routed from the RX/TX switch to the RX bandpass filter. The filter input is single-ended and the output is balanced in order to exploit the balanced nature of the RF ASIC. The band-limited signal is amplified in the internal LNA and the pre-gain amplifier before being converted to a BB signal in the passive mixer.

The gain characteristic of the BB amplifier is an amplifier with a maximum gain of 80 dB with an AGC range of 72 dB in 6dB steps.

The receiver selectivity for out-of-band signals is defined by the RF front-end SAW filter. The receiver ability to withstand large out-of-band signals is defined by the RF SAW filter and the large signal behavior of the LNA – pregain and mixer.

The inband selectivity is define by the channel filters in Mjoelner, and the in-band large signal behavior is a combination of the RF front-end and the BB amplifier large signal behavior.

AGC

Since the receiver is a linear type, the AGC must keep the BB level from the receiver within a certain range in order to stay within the dynamic range for the BB, even during fading. The AGC has to be set before each received burst with pre-monitoring or without pre-monitoring. In pre-monitoring, the receiver is switched on approximately 130µs before the burst begins. DSP measures the received signal level and adjusts AGC amplifiers via the serial bus.

RSSI must be measured accurately on range -48...-110 dBm. After the -48 dBm level, MS reports to base station the same reading.

The AGC is a combination of gain-controlled elements at both RF and BB frequencies.

It is the LNA in RF that is used as an AGC element with one step. The AGC step size of the LNA will have different values between 900 MHz and 1800 MHz, as well as across the band.

In BB the AGC has 12 steps, a combination of DCN_1 and AGC, with a resolution of ~6 dB, giving a total BB AGC range of 72 dB.

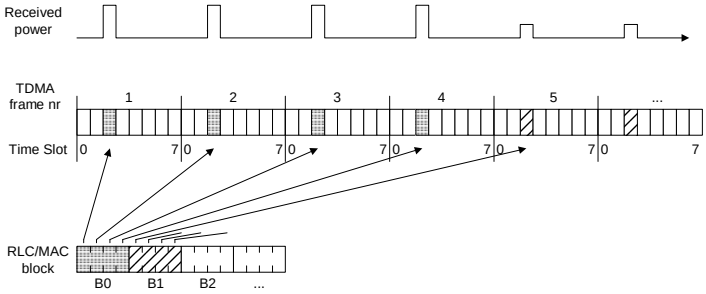
GPRS Requirements

GPRS Dual Slot

RX

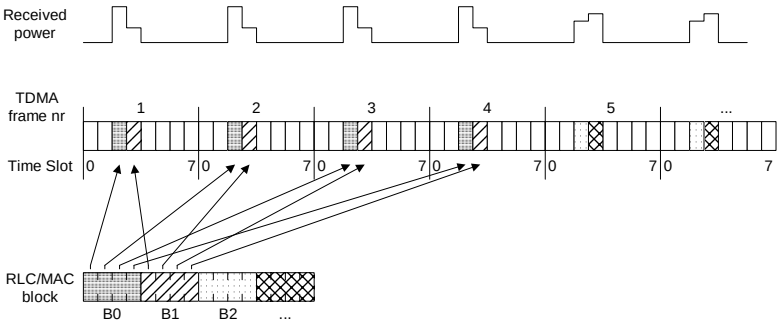
The power level transmitted by the base station will not be the same in all RX slots seen from the mobile phone. Each block interleaved on four time slots will be transmitted on the same level from the base station. In single RX slot operation, this means that four successive time slots will receive a signal on the same level if we ignore fading. The following block (four time slots) can then change up to 6 dB – even if the second package (block) is for the same mobile phone.

Figure 14: Single RX slot operation



The 6 dB step is also seen in dual slot operation. Here the change can be seen between two neighbor slots.

Figure 15: Dual RX slot operation



TX

The NPM-8 support Class 4 GPRS uses one TX slot. This means that there is no difference between normal GSM and the GRPS on the transmitter.

Synthesizer

The synthesizer requirements in GPRS are equivalent to HSCSD requirements and are limited to faster PLL settling time compared to single-slot operation.

RF Characteristics

Channel numbers and frequencies

Table 30: Channel number relative frequencies

System	Channel number	TX frequency	RX frequency	Unit
GSM850	128 <= n <= 251	F = 824.2 + 0.2 * (n –128)	F = 869.2 + 0.2 * (n -128)	MHz
GSM1900	512 <= n <= 810	F = 1850.2 + 0.2 * (n-512)	F = 1930.2 + 0.2 * (n-512)	MHz

Main RF characteristics

Table 31: Main RF characteristics

Item	GSM 850 values	GSM 1900 values
Receiver frequency range	869...894 MHz	1930...1990 MHz
Transmit frequency range	824...849 MHz	1850...1910 MHz
Duplex spacing	45 MHz	
Channel spacing	200 KHz	200 KHz
Number of RF channels	174	374
Power class	4 (2 W peak)	1 (1 W peak)
Number of power levels	15	16

Transmitter characteristics

Table 32: Transmitter main characteristics

Item	GSM 850 values	GSM 1900 values
Type	Direct conversion, nonlinear, FDMA/TDMA	Direct conversion, nonlinear, FDMA/TDMA
LO frequency range	3296.8...3395.2 MHz	3700.4... 3819.6 MHz
Output power	2 W peak	1 W peak
Gain control range	Min. 30 dB	Min. 30 dB
Maximum phase error (RMS/peak)	Max 5 deg RMS / max 20 deg Peak	Max 5 deg RMS / max 20 deg Peak

Output power requirements GSM850

Table 33: Output power requirements, GSM850

Parameter	Min	Typ	Max	Unit/Notes
Max output power		33.0		DBm
Output power tolerance (power level 5)			+/- 2.0	dB, normal cond.
Output power tolerance (power levels 6...15)			+/- 3.0	dB, normal cond.
Output power tolerance (power levels 16...19)			+/- 5.0	dB, normal cond.
Output power control step size	0.5	2.0		dB

Output power requirements, GSM1900

Table 34: Output power requirements, GSM1900

Parameter	Min	Typ	Max	Unit/Notes
Max output power		30		dBm
Output power tolerance (power level 0)			+/- 2.0	dB, normal cond
Output power tolerance (power levels 1...8)			+/- 3.0	dB, normal cond.
Output power tolerance (power levels 9...13)			+/- 4.0	dB, normal cond.
Output power tolerance (power levels 14...15)			+/- 5.0	dB, normal cond.
Output power control step size	0.5	2.0	3.5	dB

Receiver characteristics

Table 35: Receiver characteristics

Item	GSM 850	GSM 1900
Type	Direct conversion, nonlinear, FDMA/TDMA	Direct conversion, nonlinear, FDMA/TDMA
LO frequency range	3476.8...3575.2 MHz	3860.4...3979.6 MHz
Typical 3 dB bandwidth	+/- 91 kHz	+/- 91 kHz
Sensitivity	Min. –102 dBm	Min. –102 dBm
Total typical receiver voltage gain (from antenna to RX ADC)	94 dB	94 dB
Receiver output level (RF level -95 dBm)	125 – 250 mVpp	125 – 250 mVpp
Typical AGC dynamic range	92 dB	92 dB
Accurate AGC control range	72 dB	72 dB
Typical AGC step in LNA	~30 dB	~30 dB
Usable input dynamic range	-102 ... -10 dBm	-102 ... -10 dBm
RSSI dynamic range	-110 ... -48 dBm	-110 ... -48 dBm
Compensated gain variation in receiving band	+/- 1.0 dB	+/- 1.0 dB